Advances in High Speed PCB Design for Layout Professional

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Topics

- Power Distribution System Design
- Stackup Design
- Noise Reduction Strategies
- Differential Signaling
Power Distribution Design
PDS Components and their Effective Frequency Range

<table>
<thead>
<tr>
<th>Components</th>
<th>Impedance</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMPS</td>
<td></td>
</tr>
<tr>
<td>bulk caps</td>
<td></td>
</tr>
<tr>
<td>ceramic caps</td>
<td></td>
</tr>
<tr>
<td>PCB planes</td>
<td></td>
</tr>
<tr>
<td>Devices</td>
<td></td>
</tr>
</tbody>
</table>
Capacitor Mounted Inductance is Dependent Upon Via Breakouts

Mounted inductance decreases with close spacing of power/ground vias.
Advanced Capacitors

0805 SMD

0508 SMD

MLCC

LICC

LICA
Capacitor Model

L via(s)
Often dominates

Mounted inductance of capacitor is dependent upon via size and spacing.
Capacitor Frequency Response

Impedance below SRF is dictated by C.

Impedance above SRF is dictated by L.

L is dependent upon package size and mounting structure.

Best broadband performance with largest capacitor in family.
Mounting Inductance Extraction with Transfer Impedance

\[ Z = 2\pi fL \]

When \( Z_{\text{plane}} \ll Z_L \)

Same method used with VNA for measurement of PCB impedance.
0603 Via Breakout Model
10 mil End Vias

4 mil Microvia with 10 mil pad

10 mil finished via with 25 mil pad

Mounting Inductance = 1.869nH
Total Inductance = 2.369nH
0603 Via Breakout Model
10 mil Side Vias

4 mil Microvia with 10 mil pad

10 mil finished drilled via with 25 mil pad

Mounting Inductance = 1.654 nH
Total Inductance = 2.154 nH
0603 Via Breakout Model
10 mil Side Vias At Min Spacing

4 mil Microvia with 10 mil pad

10 mil finished drilled via with 25 mil pad

30 mil drilled via spacing center-to-center

Mounting Inductance = 1.307 nH
Total Inductance = 1.807 nH
0603 Via Breakout Model
13 mil Side Vias at Min Spacing

4 mil Microvia with 10 mil pad

13 mil finished drilled via with 28 mil pad

35 mil drilled via spacing center-to-center

Mounting Inductance = 1.191 nH
Total Inductance = 1.691 nH
0603 Via Breakout Model
Four 13 mil Side Vias

4 mil Microvia with 10 mil pad

13 mil finished drilled via with 28 mil pad

35 mil drilled via spacing center-to-center

Mounting Inductance = 0.864 nH
Total Inductance = 1.364 nH
10 mil IDC 0612 Breakout

Drilled via spacing 30 mils

Microvia to drilled via pad spacing 5 mils

Mounting Inductance = 0.326 nH
Total Inductance = 0.446 nH

4 mil Microvia with 10 mil pad

10 mil finished via with 25 mil pad
IDC 0612 Via Breakout Model
13 mil Vias at Minimum Spacing

4 mil Microvia with 10 mil pad

13 mil finished drilled via with 28 mil pad

35 mil drilled via spacing center-to-center

Mounting Inductance = 0.264 nH
Total Inductance = 0.384 nH
X2Y Capacitor Mounting Pattern vs. IDC 0612

- IDC 0612
  - Outside Breakout
  - 0.498 nH

- X2Y 0603
  - Std Breakout
  - 0.446 nH

- X2Y 1206
  - Std Breakout
  - 0.366 nH
## Mounted Inductance Table

<table>
<thead>
<tr>
<th>Type</th>
<th>Finished Drill</th>
<th>Pattern</th>
<th>Mounting Inductance</th>
<th>Device Inductance</th>
<th>Total Inductance</th>
</tr>
</thead>
<tbody>
<tr>
<td>0603</td>
<td>10 mil</td>
<td>End</td>
<td>1.869 nH</td>
<td>0.500 nH</td>
<td>2.369 nH</td>
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<tr>
<td>0603</td>
<td>10 mil</td>
<td>Edge</td>
<td>1.654 nH</td>
<td>0.500 nH</td>
<td>2.154 nH</td>
</tr>
<tr>
<td>0603</td>
<td>10 mil</td>
<td>Side min space</td>
<td>1.307 nH</td>
<td>0.500 nH</td>
<td>1.807 nH</td>
</tr>
<tr>
<td>0603</td>
<td>13 mil</td>
<td>Side min space</td>
<td>1.191 nH</td>
<td>0.500 nH</td>
<td>1.691 nH</td>
</tr>
<tr>
<td>0603</td>
<td>13 mil</td>
<td>4 via side min</td>
<td>0.864 nH</td>
<td>0.500 nH</td>
<td>1.364 nH</td>
</tr>
<tr>
<td>IDC 0612</td>
<td>10 mil</td>
<td>Inside breakout min spacing</td>
<td>0.326 nH</td>
<td>0.120 nH</td>
<td>0.446 nH</td>
</tr>
<tr>
<td>IDC 0612</td>
<td>13 mil</td>
<td>Inside breakout min spacing</td>
<td>0.264 nH</td>
<td>0.120 nH</td>
<td>0.384 nH</td>
</tr>
<tr>
<td>IDC 0612</td>
<td>13 mil</td>
<td>Outside breakout min spacing</td>
<td>0.378 nH</td>
<td>0.120 nH</td>
<td>0.498 nH</td>
</tr>
<tr>
<td>X2Y 0603</td>
<td>20 mil</td>
<td>6 via pattern</td>
<td>Only total L measured</td>
<td>&lt; 0.100 nH</td>
<td>0.446 nH</td>
</tr>
</tbody>
</table>
## Capacitor Figure of Merit Table

<table>
<thead>
<tr>
<th>Type</th>
<th>Finished Drill</th>
<th>Pattern</th>
<th>FOM (relative number of caps)</th>
<th>FOM (relative number of vias)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0603</td>
<td>10 mil</td>
<td>End</td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>0603</td>
<td>10 mil</td>
<td>Edge</td>
<td>.909</td>
<td>.909</td>
</tr>
<tr>
<td>0603</td>
<td>10 mil</td>
<td>Side min space</td>
<td>.763</td>
<td>.763</td>
</tr>
<tr>
<td>0603</td>
<td>13 mil</td>
<td>Side min space</td>
<td>.714</td>
<td>.714</td>
</tr>
<tr>
<td>0603</td>
<td>13 mil</td>
<td>4 via side min</td>
<td>.576</td>
<td>1.152</td>
</tr>
<tr>
<td>IDC 0612</td>
<td>10 mil</td>
<td>Inside breakout min spacing</td>
<td>.188</td>
<td>.752</td>
</tr>
<tr>
<td>IDC 0612</td>
<td>13 mil</td>
<td>Inside breakout min spacing</td>
<td>.162</td>
<td>.648</td>
</tr>
<tr>
<td>IDC 0612</td>
<td>13 mil</td>
<td>Outside breakout min spacing</td>
<td>.211</td>
<td>.844</td>
</tr>
<tr>
<td>X2Y 0603</td>
<td>20 mil</td>
<td>6 via pattern</td>
<td>.188</td>
<td>.564</td>
</tr>
</tbody>
</table>
Degradation of IDC Performance with Thermal Relief

12 x 10 mil thermal relief shows negligible degradation in mounted inductance for IDC 0612 with 13 mil finished vias and inside breakout.

Inductance with direct connection to plane
264 nH

Inductance with thermal relief
265-267 nH
Breakouts

• Breakout describes the PCB routing transition from the balls, pads, and pins of a package or component.
  - There is a tradeoff between routing area utilization and signal integrity performance.
  • Layout artists (and most engineers) do not appreciate the impact that breakout pads, traces and vias have on signaling.
Common Breakout Regions
1 Gbps - Comparison with/without Breakouts (no Xtk)

1 inch Traces

7.254 inch traces

Red = connector and trace only
Blue = Breakout models added
Green = Breakout and SMA models added
2.5 Gbps - Comparison with/without Breakouts (no Xtk)

Red = connector and trace only
Blue = Breakout models added
Green = Breakout and SMA models added

1 inch Traces

7.254 inch traces
3.125 Gbps - Comparison with/without Breakouts (no Xtk)

Red = connector and trace only
Blue = Breakout models added
Green = Breakout and SMA models added

1 inch Traces

7.254 inch traces
5 Gbps - Comparison with/without Breakouts (no Xtk)

1 inch Traces

7.254 inch traces

Red = connector and trace only
Blue = Breakout models added
Green = Breakout and SMA models added
10 Gbps - Comparison with/without Breakouts (no Xtk)

1 inch Traces

7.254 inch traces

Red = connector and trace only
Blue = Breakout models added
Green = Breakout and SMA models added
Vias

• Form a complex transition from one layer to another in a PCB.
  - Vias exhibit strong coupling to all surrounding structures.
    • Other vias
    • Component pins
    • Other vias
    • Other vias

• Planar EDA companies have just begun modeling the via.
  - How accurate is that model and what are the assumptions?
Via Transitions
Routing

• Have you ever been surprised by how “innovative” trace routing can be?
  – There are plenty of opportunities for:
    • Increased crosstalk
    • Horrid quarter and half-wave resonances caused by stubs and misplaced mismatches.
    • Via-to-via coupling
    • Poor via design.
      – EDA tools do not know what a differential via is.
        » Create multiple differential via components, complete with unique padstacks.
Non-uniform Material Properties

- All epoxy/fiberglass laminates are subject to wide variation of $E_r$.
  - Dependent on average ratio of epoxy to fiberglass.
- All epoxy/fiberglass laminates are subject to local variation of $E_r$.
  - Dependent on local ratio of epoxy to fiberglass.
## Dielectric Properties Table - N4000-2, N4000-6, N4000-6FC

**12/19/00**

<table>
<thead>
<tr>
<th>LAMINATE</th>
<th>Construction</th>
<th>RC</th>
<th>1MHz</th>
<th>1 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.002 ± 0.0005</td>
<td>1 x 106</td>
<td>69.0%</td>
<td>3.84 ± 0.34</td>
<td>3.63 ± 0.36</td>
</tr>
<tr>
<td>0.003 ± 0.0005</td>
<td>1 x 1080</td>
<td>62.0%</td>
<td>4.00 ± 0.33</td>
<td>3.80 ± 0.34</td>
</tr>
<tr>
<td>0.004 ± 0.0005</td>
<td>1 x 2113</td>
<td>54.5%</td>
<td>4.19 ± 0.36</td>
<td>4.00 ± 0.38</td>
</tr>
<tr>
<td>0.004 ± 0.0005</td>
<td>1 x 106 + 1 x 1080</td>
<td>57.7%</td>
<td>4.11 ± 0.32</td>
<td>3.91 ± 0.34</td>
</tr>
<tr>
<td>0.004 ± 0.0005</td>
<td>1 x 2116</td>
<td>43.0%</td>
<td>4.54 ± 0.54</td>
<td>4.37 ± 0.57</td>
</tr>
<tr>
<td>0.005 ± 0.0005</td>
<td>1 x 106 + 1 x 2113</td>
<td>52.8%</td>
<td>4.24 ± 0.34</td>
<td>4.05 ± 0.36</td>
</tr>
<tr>
<td>0.005 ± 0.0005</td>
<td>1 x 2116</td>
<td>51.8%</td>
<td>4.26 ± 0.35</td>
<td>4.08 ± 0.37</td>
</tr>
<tr>
<td>0.005 ± 0.0005</td>
<td>1 x 1080 + 1 x 2113</td>
<td>52.2%</td>
<td>4.25 ± 0.32</td>
<td>4.06 ± 0.34</td>
</tr>
<tr>
<td>0.006 ± 0.0005</td>
<td>1 x 106 + 1 x 2116</td>
<td>50.8%</td>
<td>4.29 ± 0.33</td>
<td>4.11 ± 0.35</td>
</tr>
<tr>
<td>0.006 ± 0.0005</td>
<td>2 x 2113</td>
<td>43.5%</td>
<td>4.52 ± 0.33</td>
<td>4.35 ± 0.46</td>
</tr>
<tr>
<td>0.006 ± 0.0075</td>
<td>1 x 1500</td>
<td>41.7%</td>
<td>4.56 ± 0.57</td>
<td>4.41 ± 0.60</td>
</tr>
<tr>
<td>0.007 ± 0.0075</td>
<td>2 x 2113</td>
<td>49.6%</td>
<td>4.33 ± 0.39</td>
<td>4.14 ± 0.41</td>
</tr>
<tr>
<td>0.008 ± 0.0075</td>
<td>1 x 7628</td>
<td>44.4%</td>
<td>4.49 ± 0.44</td>
<td>4.32 ± 0.47</td>
</tr>
<tr>
<td>0.008 ± 0.0075</td>
<td>2 x 2116</td>
<td>43.0%</td>
<td>4.54 ± 0.46</td>
<td>4.37 ± 0.49</td>
</tr>
<tr>
<td>0.008 ± 0.0075</td>
<td>1 x 2116 + 1 x 2113</td>
<td>49.6%</td>
<td>4.36 ± 0.38</td>
<td>4.18 ± 0.40</td>
</tr>
<tr>
<td>0.008 ± 0.0075</td>
<td>1 x 7629</td>
<td>42.6%</td>
<td>4.55 ± 0.47</td>
<td>4.38 ± 0.50</td>
</tr>
<tr>
<td>0.009 ± 0.0075</td>
<td>2 x 2116</td>
<td>47.8%</td>
<td>4.38 ± 0.37</td>
<td>4.20 ± 0.39</td>
</tr>
<tr>
<td>0.010 ± 0.001</td>
<td>2 x 2116</td>
<td>51.8%</td>
<td>4.26 ± 0.35</td>
<td>4.08 ± 0.37</td>
</tr>
<tr>
<td>0.010 ± 0.001</td>
<td>1 x 7628 + 1 x 1080</td>
<td>45.0%</td>
<td>4.47 ± 0.44</td>
<td>4.29 ± 0.47</td>
</tr>
<tr>
<td>0.010 ± 0.001</td>
<td>1 x 7635</td>
<td>47.5%</td>
<td>4.39 ± 0.41</td>
<td>4.21 ± 0.43</td>
</tr>
<tr>
<td>0.012 ± 0.001</td>
<td>2 x 1080 + 1 x 7628</td>
<td>45.5%</td>
<td>4.46 ± 0.40</td>
<td>4.28 ± 0.43</td>
</tr>
<tr>
<td>0.014 ± 0.001</td>
<td>2 x 7628</td>
<td>38.8%</td>
<td>4.69 ± 0.48</td>
<td>4.53 ± 0.51</td>
</tr>
</tbody>
</table>

Courtesy of ParkNelco 2002
FR4 Material Cross Section

Fiberglass
Bundles
Er = 6.6

Epoxy
Er 3.6

Non-homogeneous material has dielectric constant variation due to ratio of glass to epoxy.
Cross Section Top View

Courtesy of Isola Laminates
Fabrication Issues

- Impedance is dependent upon:
  - Trace width
    - Controlled by etch process
  - Dielectric thickness
    - Controlled by material thickness, temperature and pressure.
    - Altered by local trace density
  - Global and local Er
  - Orientation of trace relative to weave
    - Up to +/- 4% variation due to directionality.
Board Impedance - Z0
Multiple boards

• If using a backplane
  - Backplane Z0 should be 10%-7.5% tolerance
    • Increased tolerance at backplane reduces reflections.
Common Board Parameters

\[ Z_0 = \sqrt{\frac{L_0}{C_0}} \]

\[ v = \sqrt{\frac{1}{L_0 \times C_0}} \]

- \( Z_h \) 50 to 80 Ohms
- \( v \) 135 to 210 ps/inch
- \( v \) 55 to 80 ps/cm
- \( v \) is constant (\( E_r \))
  - so \( L_0 \) and \( C_0 \)
Impedance Control

• Trace impedance is controlled by:
  – Signal conductor width.
    • Secondarily by adjacent trace spacing.
  – Height above plane.
  – Dielectric constant (E_r) of material.

• FR-4 E_r = 3.4 to 4.8
  – Depends upon resin content.
  – Large range across multiple materials.
  – Smaller range across one PCB.
    » Local variations in glass/resin ratio.
Impedance Sensitivity Analysis

- Used to determine maximum impedance variation across manufacturing tolerances
  - Dielectric constant
  - Track width
    - Track spacing also for differential pair traces
  - Track height above plane
  - $E_r, W, S, H$
Impedance Sensitivity Analysis
Example for Stripline

• Calculations performed with Ansoft Transmission Line Designer in Serenade SV

• Assumptions
  - FR-4 – Er = 3.8 to 4.2 variation across board.
    • Fabrication process is adjusted to correct for actual nominal material dielectric constant.
  - Etch width tolerance is held to +/- 0.5mil (+/- 0.0127 mm).
  - Stripline dielectric thickness tolerance = +/- 1mil (+/- 0.0254 mm).
  - Trace is perfectly centered between plane layers.
    • Always some offset in manufacturing.
Diagram of Assumed Stripline Tolerances

Height

Width

Er
# Stripline Sensitivity

## 4 mil (0.1 mm), 50 ohm

## Total Sensitivity due to all tolerances

<table>
<thead>
<tr>
<th>Corner</th>
<th>Width (mils)</th>
<th>Height (mils)</th>
<th>Er</th>
<th>Impedance</th>
<th>% of Nominal</th>
<th>Max Variation</th>
<th>Delta Variation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum</td>
<td>3.5</td>
<td>11.5</td>
<td>3.8</td>
<td>57.2</td>
<td>114.40%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nominal</td>
<td>4</td>
<td>10.5</td>
<td>4</td>
<td>50.1</td>
<td>100.20%</td>
<td>14.40%</td>
<td>13.58%</td>
</tr>
<tr>
<td>Minimum</td>
<td>4.5</td>
<td>9.5</td>
<td>4.2</td>
<td>43.62</td>
<td>87.24%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
# Stripline Sensitivity (4mil)

## Sensitivity due to Er Variation

<table>
<thead>
<tr>
<th>Corner</th>
<th>Width (mils)</th>
<th>Height (mils)</th>
<th>Er</th>
<th>Impedance</th>
<th>% of Nominal</th>
<th>Max Variation</th>
<th>Delta Variation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum</td>
<td>4</td>
<td>10.5</td>
<td>3.8</td>
<td>51.4</td>
<td>102.80%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nominal</td>
<td>4</td>
<td>10.5</td>
<td>4</td>
<td>50.1</td>
<td>100.20%</td>
<td>2.80%</td>
<td>2.50%</td>
</tr>
<tr>
<td>Minimum</td>
<td>4</td>
<td>10.5</td>
<td>4.2</td>
<td>48.9</td>
<td>97.80%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Sensitivity due to Width Variation

<table>
<thead>
<tr>
<th>Corner</th>
<th>Width (mils)</th>
<th>Height (mils)</th>
<th>Er</th>
<th>Impedance</th>
<th>% of Nominal</th>
<th>Max Variation</th>
<th>Delta Variation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum</td>
<td>3.5</td>
<td>10.5</td>
<td>4</td>
<td>53.1</td>
<td>106.20%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nominal</td>
<td>4</td>
<td>10.5</td>
<td>4</td>
<td>50.1</td>
<td>100.20%</td>
<td>6.20%</td>
<td>5.60%</td>
</tr>
<tr>
<td>Minimum</td>
<td>4.5</td>
<td>10.5</td>
<td>4</td>
<td>47.5</td>
<td>95.00%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Sensitivity due to Height Variation

<table>
<thead>
<tr>
<th>Corner</th>
<th>Width (mils)</th>
<th>Height (mils)</th>
<th>Er</th>
<th>Impedance</th>
<th>% of Nominal</th>
<th>Max Variation</th>
<th>Delta Variation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum</td>
<td>4</td>
<td>11.5</td>
<td>4</td>
<td>52.7</td>
<td>105.40%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nominal</td>
<td>4</td>
<td>10.5</td>
<td>4</td>
<td>50.1</td>
<td>100.20%</td>
<td>5.40%</td>
<td>5.40%</td>
</tr>
<tr>
<td>Minimum</td>
<td>4</td>
<td>9.5</td>
<td>4</td>
<td>47.3</td>
<td>94.60%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
# Stripline Sensitivity

5 mil (0.125 mm, 50 ohm)

## Total Sensitivity due to all tolerances

<table>
<thead>
<tr>
<th>Corner</th>
<th>Width (mils)</th>
<th>Height (mils)</th>
<th>Er</th>
<th>Impedance</th>
<th>% of Nominal</th>
<th>Max Variation</th>
<th>Delta Variation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum</td>
<td>4.5</td>
<td>13.6</td>
<td>3.8</td>
<td>56.2</td>
<td>112.40%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nominal</td>
<td>5</td>
<td>12.6</td>
<td>4</td>
<td>50.17</td>
<td>100.34%</td>
<td>12.40%</td>
<td>11.62%</td>
</tr>
<tr>
<td>Minimum</td>
<td>5.5</td>
<td>11.6</td>
<td>4.2</td>
<td>44.58</td>
<td>89.16%</td>
<td></td>
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</table>
# Stripline Sensitivity

8 mil (0.2 mm), 50 ohm

<table>
<thead>
<tr>
<th>Corner</th>
<th>Width (mils)</th>
<th>Height (mils)</th>
<th>Er</th>
<th>Impedance</th>
<th>% of Nominal</th>
<th>Max Variation</th>
<th>Delta Variation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum</td>
<td>7.5</td>
<td>19.6</td>
<td>3.8</td>
<td>54.3</td>
<td>108.60%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nominal</td>
<td>8</td>
<td>18.6</td>
<td>4</td>
<td>49.91</td>
<td>99.82%</td>
<td>8.60%</td>
<td>8.50%</td>
</tr>
<tr>
<td>Minimum</td>
<td>8.5</td>
<td>17.6</td>
<td>4.2</td>
<td>45.8</td>
<td>91.60%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Stripline Manufacturing Sensitivity

Manufacturing Sensitivity

Impedance Variation From Nominal 50 Ohms

Nominal Trace Width

4 mil 5mil 8 mil
Return Loss From Impedance Discontinuity

Reflection boundaries form resonant frequency.

50 Ohm 1 inch (25mm) Discontinuity 50 Ohm
Reflection Coefficient

• At a boundary between transmission line discontinuities a reflection occurs.

• The reflection coefficient can be defined as:

$$\Gamma = \frac{R_{\text{dis}} - Zo}{R_{\text{dis}} + Zo}$$

- Where $\Gamma$ is the reflection coefficient.
- $Zo$ is the impedance of the incoming line.
- $Z_{\text{dis}}$ is the impedance of the discontinuity.
Reflection Coefficient

\[ \Gamma = \frac{R_{\text{dis}} - Z_0}{R_{\text{dis}} + Z_0} \]

\( \Gamma \) is how much signal will be reflected when it hits \( R_{\text{dis}} \).

\( R_{\text{dis}} \) is anywhere there is a discontinuity.
Reflection Coefficient (Magnitude Return Loss)

\[ \Gamma = \frac{R_{\text{dis}} - Z_0}{R_{\text{dis}} + Z_0} \]

\( \Gamma \) for a -10% discontinuity is -0.053
\( \Gamma \) for a +10% discontinuity is +0.048

\( R_{\text{dis}} \) is anywhere there is a discontinuity.

\[ Zo \rightarrow R_{\text{dis}} \rightarrow Zo \rightarrow RL \]
Return Loss Magnitude From Impedance Discontinuity

+/-15% impedance tolerance
+/-13.6% 4 mil trace
+/-11.6% 5 mil trace
+/-8.5% 8 mil trace

2.77 GHz resonance across 180 ps discontinuity
Return Loss From Two Impedance Discontinuities

Reflection boundaries form multiple resonance frequencies.

50 Ohm 50 Ohm

1 inch (25mm) Discontinuity 1 inch (25mm) Discontinuity

50 Ohm
Return Loss Magnitude From Impedance Discontinuity of (4 mil) ±13.6% 4 mil trace
0.241 (-12.4 dB)

Multiple resonance points across discontinuities
Maximum Return Loss Vs. Track Width

Return Loss vs. Impedance Tolerance

Impedance Variation From Nominal

Return Loss

-25
-20
-15
-10
-5
0

5.00% 7.00% 9.00% 11.00% 13.00% 15.00%

Max Return Loss
Noise Reduction Techniques
PCB Power Noise

- Power supply noise is caused by three phenomena.
  - Delta I semiconductor core switching transients that draw from planes.
  - Delta I semiconductor driver switching transients.
  - Parallel-plate mode conversion due to via power injection into inter-plane layers.
Methods to Reduce Noise

- Always pair power and ground planes.
  - Use thinnest dielectric spacing possible.
    - Use buried capacitance layers designed for power systems.
- Use only one capacitor value for high-frequency decoupling.
  - Largest value in package with smallest inductance.
    - Evenly distribute capacitors across entire area of power planes to reduce overall impedance.
Ground Bounce vs. other noise

- Ground bounce, or reference bounce, is due to delta I noise across packages and boards of high impedance.
- There is absolutely nothing that a PCB designer can do to reduce the “ground bounce” of a poorly designed device package.
- A designer can reduce power plane noise though good stackup and good decoupling practices.
Speed 2000 Power Plane Simulations 4-layer Board

3D Noise Displayed Over Time
Speed 2000 Power Plane Simulations 4-layer Board

Peak Noise 3D Display

Peak Noise Gradient Display
AMD Processor Board with decoupling 1000ps risetime
AMD Processor Board with decoupling capacitors 200ps risetime
Reducing Switching Noise

- Reference all high speed signals and clocks to ground on all layers.
  - Use power referenced layers for slow speed or static signals.
- Place two to four ground vias on each side of clock via transitions.
- Place one ground via per three high speed signal vias within bus layer transitions.
- Never cross a plane split on an adjacent layer.
- Place decoupling capacitors on the periphery of all high speed components.
Spilt Planes (top view)

Trace Crossing a Split Plane
Top View
Split Planes
(cross-section)

Trace Crossing a Split Plane
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Split Plane RF Return Path

- Power Plane
- Ground Plane
- Trace
- Slot Wave
Split Planes and RF Return Path

• At a split in a plane, the RF return path is broken.
  - This is the instantaneous current path formed by moving electric and magnetic fields between the trace and the underlying plane.
  - The signal currents continue to flow, but the planar currents are broken.
    • When these planar currents are broken, a slot mode is formed, where some of the energy flows through the slot between the two planes.
    • Current is injected into the planes to support the slot mode.
    • Interplanar capacitance may mitigate the effect, but with increased power system noise.
Noise Injection Through Via Transitions

Lack of an RF return path causes parallel plate waves to be injected into the power system.

Power planes provide the current return path.

The return path power injection causes noise on the planes with harmonics of the signal switching rate.
Noise Suppression by Return Path Control

Addition of capacitors near the via transition site, across the board, and at the edge of the board, help to support a good RF return path.

The capacitor vias, themselves, are a component of the mutual return path, due to coupling with the signal vias.

Place several decoupling capacitors around all high-speed clock signal vias to support the return path, decrease noise and EMI.

If ground referenced signals are used throughout, then ground vias should surround all high-speed signals, in place of capacitors.

2 ground via per clock via.

1 ground via per high speed signal via.
Ground vias are used to surround high speed clock via for noise containment.
Ground/VCC Plane Separation

- $C_{\text{plane}} = 0.225 \, \text{pF/in} \times \varepsilon_r \times \frac{A}{T}$
  - $\varepsilon_r$ = dielectric constant
  - $A$ = area of plane in inches$^2$
  - $T$ = thickness of dielectric between planes

  - Plane capacitance decreases linearly with $T$

- $L_{\text{plane}} = 32 \, \text{pH/mil} \times T$ per square

  - Plane inductance increases linearly with $T$
Ground/VCC Plane Separation

- Since power plane capacitance is a linear function of separation, and power plane inductance is a linear function of separation, power plane impedance decreases linearly with decreased plane spacing.
  - Whenever power plane spacing is reduced by a 2X, signal switching noise is reduced by a factor of 2.
- Due to low capacitance between planes, noise below 100 MHz is not significantly reduced.

- Buried capacitance layers are normally not necessary, as long as:
  - PDS is designed sufficiently to 100 MHz Ztarget.
  - High speed signal return paths are managed.
Split Planes and RF Return Path

• At a split in a plane, the RF return path is broken.
  – This is the instantaneous current path formed by moving electric and magnetic fields between the trace and the underlying plane.
  – The signal currents continue to flow, but the planar currents are broken.
    • When these planar currents are broken, a slot mode is formed, where some of the energy flows through the slot between the two planes.
    • Current is injected into the planes to support the slot mode.
    • Interplanar capacitance may mitigate the effect.
Split Planes and the RF Return Path (cont.)

- The slot mode effect can be decreased by providing an underlying ground plane the “absorbs” the slot mode energy.
  - The capacitance between the power planes and the ground plane provide closure of the return path.
Split Planes and the RF Return Path (cont.)

- Slot mode waves can also be mitigated by decreasing the slot separation between the two planes.
  - Decreasing the separation increases the capacitance between the power planes.
    - Decreases the coupled energy.
    - Decreases the slot impedance.
    - Decreases the crosstalk to distant traces.
Split Plane Layout Rules

- Always place a ground plane under the split power planes.
  - Reduce inter-plane spacing to the minimum allowed by materials and manufacturing rules.
    - Smaller is better. (4 mil, 3 mil.)
  - Reduce the size of the slot (gap) between planes to the minimum allowed by manufacturing.
  - Place only “slow” signals across the split.
  - DO NOT PLACE “external” interface signals across the slot.
    - Signals that attach to external box connectors.
Important Interconnect Characteristics – Crosstalk

- Crosstalk is the most neglected component in backplane system design.
  - Modeled well
    - Crosstalk in traces.
      - 2D solvers easily model these elements
    - Crosstalk in connectors
      - 2D and 3D approaches used by manufacturers
      - Generally well modeled
      - Boundary of model is often not well defined or thought out.
  - Often modeled poorly
    - Device packages
    - Package breakouts
    - Connector via fields.
Connector
SLM
Connector Crosstalk
1:1 Signal to Ground
Connector Crosstalk
2:1 Signal to Ground Electric Field
Connector Crosstalk
9:1 Signal To Ground
Bandwidth

• The quest for higher system performance, is the quest for higher bandwidth.
• It is the bandwidth of system components that limit data rates.
• This concept of bandwidth is tightly tied to the concepts of risetime, frequency, bit rate, and modulation.
Rise Time vs. Frequency vs. Bit Rate vs. Bandwidth

- **Rise time** – The time for a signal to transition from 10% to 90% of full swing.
- **Frequency** – The rate of repetition of a signal.
- **Bit Rate** – The number of data bits per second transmitted or received.
- **Bandwidth** – The “space” required for the signal.
  - Dependent upon rise time, frequency, bit rate and encoding of the signal.
- **Modulation** – The encoding used to transmit the signal.
  - Binary uses 2 values per bit.
  - PAM-4 uses 4 values per bit.
Digital Data Bit Rate

- Digital data is usually encoded as a binary data stream
  - binary = 2 states ("one" and "zero")
- For binary encoding the bit rate is twice the frequency of transitions of the bits.

\[
\text{Frequency} = \frac{1}{\text{period}}
\]
Digital Data Bit Rate

- Bandwidth is dependent upon:
  - Frequency of data stream
  - Rise time of the pulse edges
    - Faster data and edge rates require more bandwidth.
Risetime/Bandwidth

- For digital pulse trains the maximum bandwidth required can be approximated by the following formula:

\[
\text{Bandwidth} = \frac{0.35}{\text{Risetime}}
\]

This is true no matter what the frequency of the signal is!

But, it is only an approximation!!!
# Logic Family Speed Chart

<table>
<thead>
<tr>
<th>Logic Family</th>
<th>Rise/Fall Time</th>
<th>Equivalent Edge Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>ORIGINAL CMOS</td>
<td>60 ns</td>
<td>6 MHz</td>
</tr>
<tr>
<td>TTL, HCMOS</td>
<td>11 ns</td>
<td>32 MHz</td>
</tr>
<tr>
<td>LS TTL</td>
<td>5.5 ns</td>
<td>64 MHz</td>
</tr>
<tr>
<td>FCT</td>
<td>&lt;1 ns</td>
<td>&gt;350 MHz</td>
</tr>
<tr>
<td>ECL 100K</td>
<td>&lt;1 ns</td>
<td>&gt;350 MHz</td>
</tr>
<tr>
<td>3.3V CMOS</td>
<td>0.5 ns</td>
<td>700 MHz</td>
</tr>
<tr>
<td>0.35(\mu) CMOS ASIC</td>
<td>0.3 ns</td>
<td>1200 MHz</td>
</tr>
<tr>
<td>0.18(\mu) CMOS</td>
<td>0.2 ns</td>
<td>&gt;1750 MHz</td>
</tr>
<tr>
<td>3.125 Gbps Serdes</td>
<td>0.050 ns</td>
<td>7000 MHz</td>
</tr>
<tr>
<td>10 Gbps Serdes</td>
<td>0.025 ns</td>
<td>14000 MHz</td>
</tr>
</tbody>
</table>
Differential Signaling
Differential Signals

- **Definitions:**
  - **Differential signal** – signal driven on two lines with opposite voltage (current) direction.
  - **Single-ended** – signal driven on one line.
  - **Common mode** – current on two lines traveling in the same direction.
    - **Even mode** – the common mode wave traveling down one line
  - **Differential mode** – current on two lines traveling in opposite directions.
    - **Odd mode** – the differential mode wave traveling down one line.
Common-mode Drive
Differential Drive
Single-ended vs. Differential

- The impedance of a pair of traces can be broken down into two modes:
  - Even Mode
    - Current is driven in the same direction
  - Odd Mode
    - Current is driven in the opposite direction
- All coupled lines have multiple modes, depending upon the switching patterns.
  - Differential signaling uses a controlled mode which has unique properties
Impedance of Wire Pairs

The impedance of a pair of wires can be described as a matrix of impedance values which can be extracted using a field solver.

\[
Z = \begin{bmatrix}
Z_{11} & Z_{12} \\
Z_{21} & Z_{22}
\end{bmatrix}
\]

Z_{11} and Z_{22} are called the self impedances.

Z_{21} and Z_{12} are called the mutual impedances.
Even Mode vs Odd Mode

- The impedance of a symmetric system of two lines for the two modes is defined as follows:

\[ Z_{11} = Z_{22} \]
\[ Z_{12} = Z_{21} \]
\[ Z_{even} = Z_{11} + Z_{12} \]
\[ Z_{odd} = Z_{11} - Z_{12} \]
\[ Z_{common} = \frac{1}{2} Z_{even} \]
\[ Z_{diff} = 2Z_{odd} \]
Differential Facts

• All coupled traces have even and odd mode impedances.
  - Even mode impedance is > than odd mode.
  - For weakly coupled lines that are far apart, the even mode impedance is almost equal to the odd mode impedance.

• As traces are closely coupled, the odd mode impedance lowers and the even mode impedance raises.
Differential Propagation

• Signals launched differentially will propagate in the odd mode.
  – But no signal is truly differential!
    • Skew due to driver.
    • Skew due to package and PCB.
    • Skew can be decomposed into even and odd modes.

• Signals launched single-ended will propagate in both the even and odd modes, depending upon the specific data patterns.
Differential Skew

• Since differential skew always occurs, it must be controlled.

• Rule of thumb:
  - For good signal quality at receiver, differential skew should never exceed the following:
    • 10 Gbps - about 10 mils (0.254 mm)
    • 3.2 Gbps - about 20 mils (0.508 mm)
    • 2.5 Gbps - about 25 mils (0.635 mm)
    • 1 Gbps - about 50 mils (1.27 mm)
    • 622 Mbps - about 100 mils (2.54 mm)
Differential Design Tradeoffs

- Loosely coupled
  - better impedance control
  - less sensitivity to manufacturing variations
  - lower track density
  - lower even mode return loss
  - lower insertion loss
  - less impedance variation at 2mm connector transitions
  - less impedance variation at BGA escape transitions
  - less impedance variation at via transitions
Differential Design Tradeoffs

- Tightly coupled
  - worse impedance control
  - greater sensitivity to manufacturing variations
  - higher track density
  - higher even mode return loss
  - higher insertion loss
  - greater impedance variation at 2mm connector transitions
  - greater impedance variation at BGA escape transition
  - greater impedance variation at via transitions
## Attenuation of PCB traces

### Total Loss at Switching Rates (50 Ohm Stripline, 20 inches (508 mm) trace length)

<table>
<thead>
<tr>
<th></th>
<th>5 Gbps</th>
<th>6.250 Gbps</th>
<th>10 Gbps</th>
<th>20 Gbps</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Signaling Rate (PAM-4)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Signaling Rate (PAM-2)</strong></td>
<td>622 Mbps</td>
<td>1 Gbps</td>
<td>2.5 Gbps</td>
<td>3.125 Gbps</td>
</tr>
<tr>
<td><strong>Fundamental Frequency</strong></td>
<td>100 MHz</td>
<td>311 MHz</td>
<td>500 MHz</td>
<td>1.25 GHz</td>
</tr>
<tr>
<td>Trace width</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 mil (0.1mm)</td>
<td>0.906</td>
<td>1.776</td>
<td>2.388</td>
<td>4.37</td>
</tr>
<tr>
<td>5 mil (0.127 mm)</td>
<td>0.784</td>
<td>1.558</td>
<td>2.114</td>
<td>3.936</td>
</tr>
<tr>
<td>8 mil (0.2 mm)</td>
<td>0.582</td>
<td>1.204</td>
<td>1.664</td>
<td>3.226</td>
</tr>
<tr>
<td>10 mil (0.254 mm)</td>
<td>0.502</td>
<td>1.064</td>
<td>1.486</td>
<td>2.944</td>
</tr>
</tbody>
</table>

6 dB attenuation = 50% signal attenuation

Computed with Ansoft Transmission Line Designer in Serenade SV
# Attenuation of Traces Due to Conductor Skin Effect

## Conductor Loss at Switching Rates (50 Ohm Stripline)

<table>
<thead>
<tr>
<th>Trace width</th>
<th><strong>5 Gbps</strong></th>
<th><strong>6.250 Gbps</strong></th>
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<th><strong>20 Gbps</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>4 mil</td>
<td>0.776</td>
<td>1.372</td>
<td>1.74</td>
<td>2.752</td>
</tr>
<tr>
<td>5 mil</td>
<td>0.654</td>
<td>1.156</td>
<td>1.466</td>
<td>2.318</td>
</tr>
<tr>
<td>8 mil</td>
<td>0.454</td>
<td>0.802</td>
<td>1.018</td>
<td>1.608</td>
</tr>
<tr>
<td>10 mil</td>
<td>0.374</td>
<td>0.66</td>
<td>0.838</td>
<td>1.326</td>
</tr>
</tbody>
</table>

**3 dB attenuation = 30% signal attenuation**

**6 dB attenuation = 50% signal attenuation**

Computed with Ansoft Transmission Line Designer in Serenade SV
## Attenuation of Traces Due to Dielectric Loss \((0.014 \tan \Delta)\)

### Dielectric Loss at Switching Rates (50 Ohm Stripline)

<table>
<thead>
<tr>
<th></th>
<th>5 Gbps</th>
<th>6.250 Gbps</th>
<th>10 Gbps</th>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 mil</td>
<td>0.13</td>
<td>0.402</td>
<td>0.648</td>
<td>1.618</td>
</tr>
<tr>
<td>5 mil</td>
<td>0.13</td>
<td>0.402</td>
<td>0.648</td>
<td>1.618</td>
</tr>
<tr>
<td>8 mil</td>
<td>0.13</td>
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<td>10 mil</td>
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<td>1.618</td>
</tr>
</tbody>
</table>

**6 dB attenuation = 50% signal attenuation**

Computed with Ansoft Transmission Line Designer in Serenade SV
Hspice Simulation of Insertion Loss

20-inch trace on low-loss FR-4 material. Loss tangent = 0.014