Boundary-Scan to the Rescue: Restoring Test Access to High-Density PCBs and Systems

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Ray Dellecker ray@jtag 425-898-8968
Bob Twigg robert@jtag 206-367-1103
Brian Johnston bjohnston@pgi-solutions 503-255-9933

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Agenda

Why should we care about test?
The impact of high-density PCBs on testing
Boundary-scan to the rescue
  Overview 1149.1, PCB testing and In-System Programming
Designing for boundary-scan test
What results you can expect
Demonstration of boundary-scan testing
Why should we care about test?
Typical Testing Process

Assembly → Optical Inspection → Structural Test → Functional Test → System Test → Customer

Targeted Fault Types

- Missing parts
- Solder problems
- At-speed problems
- Configuration problems
- Process faults
- Stuck @ 0 / 1
- Device problems
- Environmental testing

The customer is not supposed to be part of the test strategy
The Testing Mission

- Principal objective: Find faults early in the production flow
- Feed results back to control the process
- Keep up with advances in technology
- Keep it cost-effective

In other words, do the (nearly) impossible:
  - Maintain production line throughput
  - Minimize capital and operating expenses
  - Assure excellent quality to the customer
Advances in PCB Technology ...

- Surface mount technology
- Multi-layer boards
- Micro-vias
- Devices on both sides
- No space or electrical margin for test points
- Ball-grid arrays with interconnects under the pkg

... a roadmap that leads to test “challenges”
Quantifying the Test Challenge

A complex PCB today can contain more than 20,000 solder joints.

As a result, even if the manufacturer achieves “world-class” quality levels (< 100 ppm structural faults), the result is --

Fault-free board yield is likely to be less than 10% !!!

Ref: Charles Robinson and Amit Verma, Teradyne Inc., APEX 2002 Conference
Testing High-Density PCBs with ICT

Faults may not be found by ICT

Requires >25 mil pad

No access to inner layers

> 50 mil spacing

Power or GND
ICT Design Rules

- Minimum test point (incl separation) = 0.050”D (and wider is better), or 0.00196 in\(^2\) per test point
- 1000 test points ~ 2 in\(^2\) lost area on the PCB
- Other considerations:
  - Provide keep-aways (protected area) around test points for tall components
  - Keep test points away from board edge
  - Try to avoid probing both sides of the board
  - Try to avoid moving test points after the fixture has been constructed

ICT Fixture Facts of Life

- Usually not available during prototype phase
- Complex PCBs = complex fixtures
- Complexity translates to high cost and low reliability, ($ thousands to tens of thousands)
- Expensive to change
- Eroding test coverage

all of which lead to...
The dreaded bone-pile
Boundary-scan to the rescue
IEEE 1149.1 Boundary-Scan Standard

- **Adopted in 1990 by the IEEE as Standard 1149.1**
  - Prepared by the Joint Test Action Group (JTAG)
  - Foresaw problems in board testing as chip design advanced

- **1149.1 is an IC standard**
  - Consists of a serial interface to the device I/Os
  - Defines a set of operations outside the chip’s normal operation

- **Semiconductor manufacturer responsible for:**
  - Designing silicon in compliance with the standard
  - Providing compliant **BSDL** file

- **Many key components comply with the Standard**
  - Microprocessors, CPLDs, ASICs, FPGAs, DSPs, etc.
  - Many PCBs have scan parts already on-board
IEEE 1149.1 Boundary-Scan Architecture

- Registers added to the IC allow data from an external source to be loaded into ... ... and read from the device pins
- Accesses a large number of electrical test points – every I/O becomes a test point
- **TAP = TDI, TDO, TMS & TCK** plus optional **TRST**

Internal Core Logic

Instruction Reg.

ID Register

TAP Controller

Bypass

Registers added to the IC allow data from an external source to be loaded into ... ... and read from the device pins

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Board Testing with Boundary-Scan

- Scan infrastructure
- Interconnections
- Non-scan clusters
- Memory clusters (address, data, & control signals)
**The Real Estate Question**

Q. How much extra space does boundary-scan require???

A. In many cases, Boundary-Scan actually saves space
   - Save 2.0 in² for every 1,000 test points eliminated
   - Plus traces no longer needed to the test points
   - Many complex devices contain boundary-scan (whether it’s being used or not) with no size penalty
   - Trade this off against minimal added space for terminations and connectors
Boundary-Scan Fault Coverage

- Finds solder bridge fault
- Checks continuity
- Finds open
- Finds stuck-at 1 or 0
- Power or GND
In-System Programming

- Eliminates handling of pre-programmed parts
  - Less damage to sensitive ICs
  - Simplifies inventory control
  - Recommended by PLD and flash vendors
- No sockets and no adapters needed
- Just-in-time programming
  - Data can be customized for finished goods
  - Easy to re-program
- High-speed production can be achieved with scan
  - Capable of demanding beat rates
  - Parallel programming arrangements
Applying boundary-scan in the factory
Production Integration

- Integrated structural testing: boundary-scan with Flying Probe, in-circuit testing, etc.
- Integrated into functional test
- Combined with system test
Integration with Structural Test

- Boundary-Scan Application Development
- Boundary-Scan Application Files
- Integrated GUI and Diagnostics
- Integrated Boundary-Scan Controller (PCI, PXI, or ISA)
- Application Execution
Integration with Functional Test

PXI Rack with Integrated Boundary-Scan Controller

Execution Sequencer

Boundary-Scan Application Development

Boundary-Scan Application Files
Integration with System Test

Observe boundary-scan results during stress testing

Boundary-Scan Application Development

Boundary-Scan Application Files

Boundary-Scan TAP cable
Designing for test
DFT Guidelines

- Check with design engineer or test engineer to determine which nets are boundary scannable nets
- Route boundary-scan TAP Signals as though they are high frequency signals; if possible do not auto-route these signals
- Consider using test nodes in place of TAP connector to save real-estate
- Blind via’s and hidden nets are permissable for nets that are boundary-scannable
- Consider using multiple chains (no loss of test coverage)
- Use pin direction whenever possible
- Suggest pullup and pulldown resistors on unterminated nets, instead of tying these nets directly to ground or Vcc
DFT Benefits

- Large reduction or elimination of test points
- Predictable test coverage, prior to layout of the board
- Fewer PCB layers, shorter path lengths, lower emissions, higher speed operation
- Tests ready for testing your prototypes
- FPGA and Flash In-circuit Programming
Board Design Simplification

(One long scan chain)

COMPLEX

TAP Connector

Buffers for Fanout

Scan devices

Jumpers to enable devices

TDO

TMS

TCK

TRST

TDI

SIMPLE

TAP Connectors

TAP SIGNALS 1

TAP SIGNALS 2

TAP SIGNALS 3

TAP SIGNALS 4

PLD

Logical groupings

Devices for Cluster and Inter. tests

Devices for Cluster and Inter. tests

FLASH Control

Each TAP will support 5 to 8 devices. Dependent on TAP signal routing and net length.
What Results You Can Expect

- Regain access for structural testing of high-density SMT boards and systems
- Simplify test fixtures while achieving high fault coverage
- Accelerate development of manufacturing tests, achieve quicker time to market
- Integrate into existing test processes
- Unified test platform for R&D, debug, manufacturing, service, and programming
- Control the bone-pile